Service Repair Documentation
Level 3 –A70_IFX

Release	Date	Department	Notes to change
R 1.0	23.03.2006	BenQ S CC CES	New document

Table of Content

1 Introduction

1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3.

1.2 Scope

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Mobile phones up to level 3.

1.3 Terms and Abbreviations

2 List of available level 3 parts

(according to Component Matrix V1.17 - check C-market for updates)

Product	RF Chipset	ID	Order Number	Description CM
A70	HIT, IFX	C204	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C230	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C368	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C369	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C370	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C371	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C372	L36377-F6105-K	CAPACITOR 1U (Cap-Type6)
A70	HIT, IFX	C373	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	C377	L36377-F6225-M	CAPACITOR 2U2 (Cap-Type4)
A70	HIT, IFX	D171	L50610-L6150-D670	IC EGOLDLITE PMB7860
A70	HIT, IFX	D361	L50645-J4682-Y55	IC ASIC SALZBURG75 TWIGO3+75
A70	IFX	D4001	L50610-L6167-D670	IC TRANCEIVER PMB6271 SMARTI SD2
A70	IFX	D4081	L50651-Z2002-A67	IC MODUL PA RF3147 (PA-Type6)
A70	HIT, IFX	N308	L50610-C6153-D670	IC V-REG 2.9V (Vr-Type2) PB Free
A70	IFX	N4071	L50645-K280-Y324	IC FEM EPCOS GSM850 1800 1900 (Fem-Type8)
A70	HIT, IFX	R106	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R141	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R201	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R204	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R205	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R221	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R222	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R295	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R371	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	IFX	R4001	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
A70	HIT, IFX	R805	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R902	L36852-C-X	RESISTOR 0R0 (Res-Type8)
A70	HIT, IFX	R955	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
A70	HIT, IFX	V151	L36840-D5062-D670	DIODE RB751S (Di-Type3)
A70	HIT, IFX	V211	L36830-C1097-D670	TRANSISTOR FDG313N (Tra-Type1)
A70	HIT, IFX	V222	L36830-C1112-D670	TRANSISTOR SI1902 (Tra-Type4)
A70	HIT, IFX	V361	L36830-C1110-D670	TRANSISTOR SI3911 (Tra-Type3)
A70	HIT, IFX	Z171	L50645-F102-Y40	QUARZ 32,768KHZ (Q-Type4)
A70	HIT, IFX	Z211	L50640-U6034-D670	FILTER EMI (Fi-Type3) PB Free
A70	IFX	Z5001	L36145-F260-Y17	QUARZ 26MHZ (Q-Type1)

3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A1)
- Troubleshooting Frame A62/A65(A70/A75) (F30032-P405-A1)
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

Reference: Equipment recommendation V2.0
(downloadable from the technical support page)

4 Required Software for Level 3

- Windows XP
- Winsui
- GRT Version 3.09 or higher
- Internet unblocking solution (JPICS)

5 Radio Part

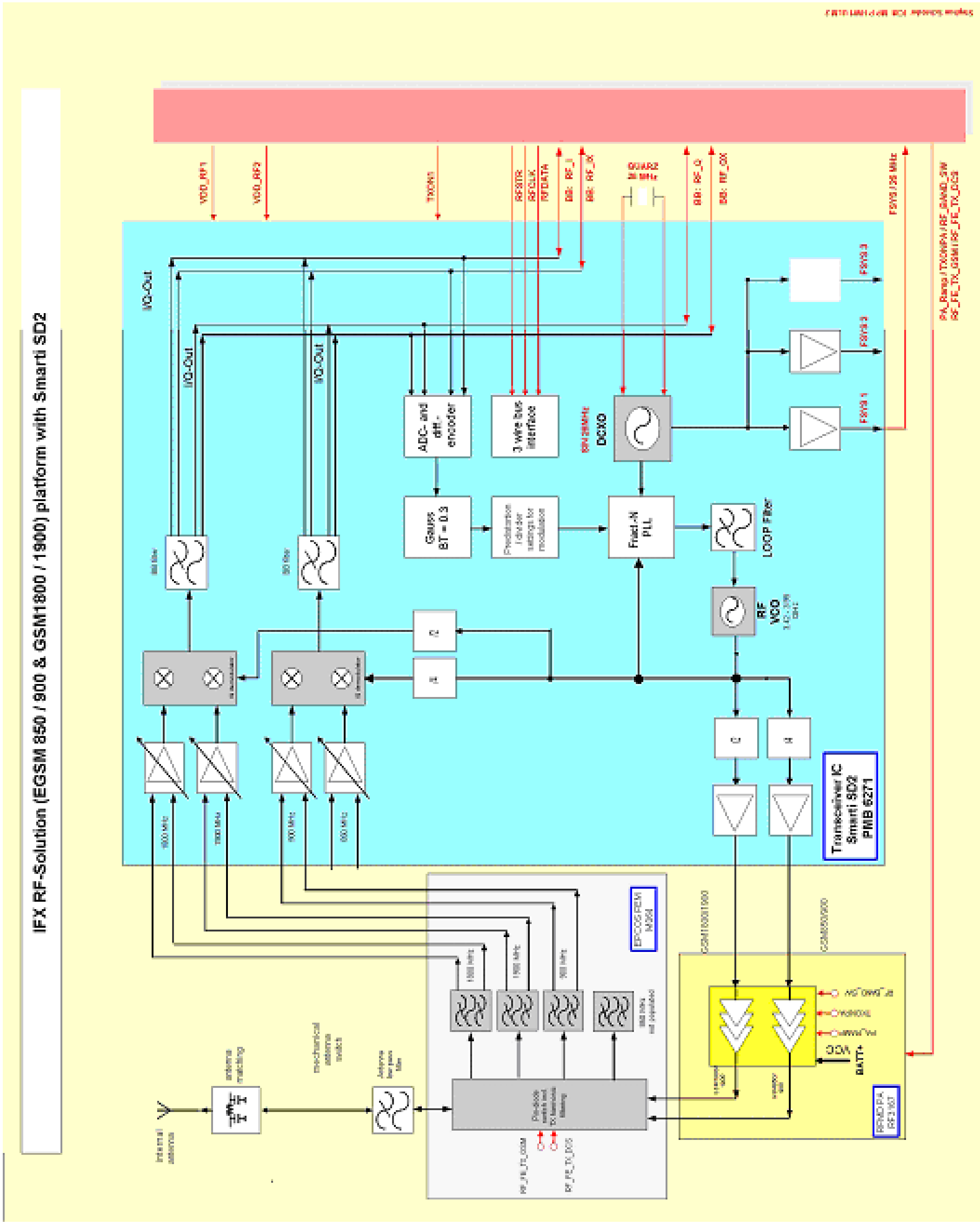
The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and fed to the A/D-converter of the logic part. In the transmission direction, the analog GMSK-signal from the baseband section is converted back to a digital signal and adapted to the following modulator. This digital modulator injects the modulation into the LO1 control loop via fast divider switching. This modulated LO1 signal is divided by 2 or 4 to get the DCS1800 / PCS1900 or GSM850/EGSM900 TX frequency. To reach the output power the signal is then amplified in the power amplifier.

The RF-part is designed for Quad band operation (GSM850, EGSM900, DCS1800, PCS1900) and consists of the following components:

- SMARTi SD2 chip set PMB6271 with the following functionality:
  - 26MHz DCXO (Digital Controlled Crystal Oscillator) reference oscillator
  - PLL for local oscillator LO1
  - Integrated loop filter for the RF synthesizer
  - LO1-VCO
  - Direct conversion receiver with channel filtering
  - Sigma Delta Modulator
- Transmitter power amplifier (PA) RF3147 (PA)
- Front-End-Module (FEM) M064 including RX-/TX-switch and GSM900/DCS1800/ PCS1900 receiver SAW-filters for international version
- Front-End-Module (FEM) M026 including RX-/TX-switch and GSM850/EGSM900/ DCS1800/PCS1900 receiver SAW-filters for LAM version

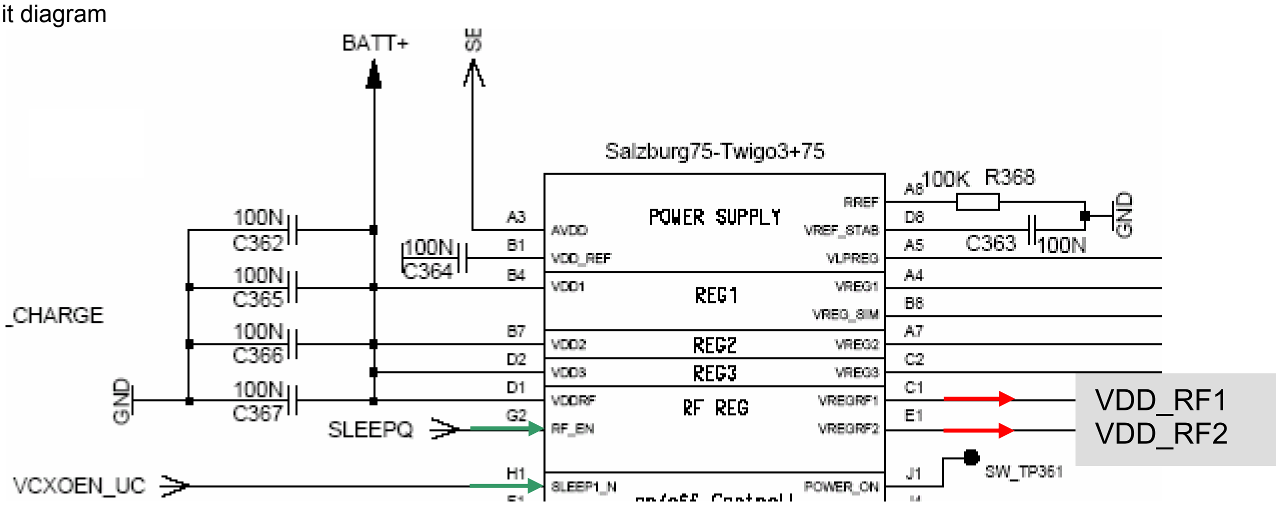
5.1 Block diagram RF part



5.2 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D361.It generates the required 2,8V “RF-operating voltages” named VDD_RF1 and VDD_RF2 for the SD2.. The voltage regulator is activated as well as deactivated via SLEEPQ (TDMA-Timer R11) and VCXOEN_UC (M4) provided by the EGOLDlite. The temporary deactivation is used to extend the stand by time.

Circuit diagram

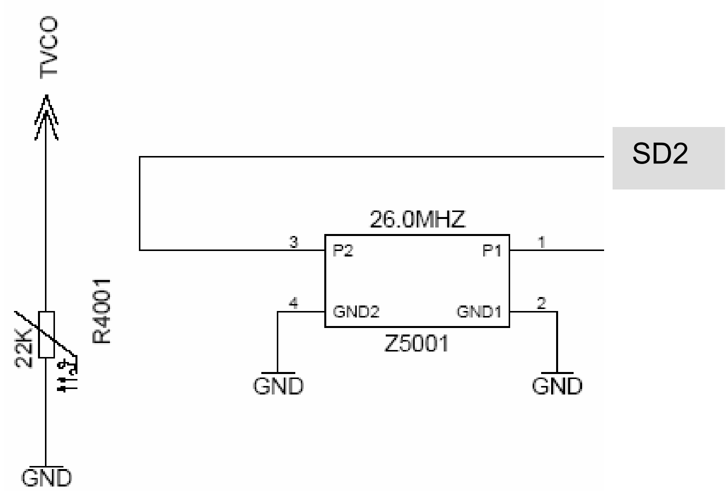


5.3 SMARTi SD2 PMB6271

5.3.1 Integrated 26MHz DCXO reference oscillator

The 26 MHz signal is created by an integrated controlled DCXO Z5001. For temperature measurements of the DCXO a temperature-dependent resistance is used R4001. The frequency of the reference oscillator can be adjusted by the baseband via three wire bus programming. Three active buffer stages are included in SMARTi SD2 to give sufficient isolation between the baseband-chip (or any other RF / BB chip) and the RF-circuit.

Circuit diagram



5.3.2 Local oscillator

The local oscillator (LO1) consists of a 23-bit fractional-N PLL and the VCO, both integrated in the SMARTi SD2 and a loop filter which is internal as well. The PD frequency is 26MHz. An LO2 is not required. The frequency range of the VCO is 3420MHz to 3980MHz for the triple-band phone GSM900/1800/1900. Therefore the LO frequency is 4 times the RX/TX frequency for GSM850/GSM 900 and 2 times RX/TX frequency for DCS1800/PCS1900.

The VCO has 1024 bands that are chosen by the 'binary automatic band select' BABS at the PLL start with the Channel 2 programming word. After the BABS the 'open loop gain adjust' OLGA sets two charge pump currents and measures the corresponding VCO frequency. So the system knows the result of a loop gain relevant parameter and adjusts the loop gain automatically by the programmable charge pump current. After this adjustment the analog locking starts. The worst case specified lock time is 200µs. So the synthesizer is capable of GPRS class 12. Due to the automatic band select with the fine VCO bands the tune voltage stays normally quite constant over the channels which enlarges the KVCO flatness.

The GMSK modulation for TX is injected by adapting the divider value of the PLL very fast to get the desired modulation. The time constant of the internal loop filter is measured before each burst as well and tolerances are compensated to get a good modulation.

5.3.3 Receiver

The SMARTi SD2 consists of a direct conversion receiver for GSM850/900/1800/1900. The GSM850/900/1800/1900 LNAs with balanced inputs are integrated into the chip. The LNA gain is switchable. For the "High Gain" state the mixers are optimised for conversion gain and noise figure, in the "Low Gain" state the mixers are optimised to large signal behaviour for operation at a high input level. The gain step for the LNA is approximately 34dB for all four bands. There is another fixed gain precision amplifier with 6dB that will be switched on at reference sensitivity level (-90dBm input level) to avoid accuracy losses at very low input levels.

A quadrature demodulator converts the amplified RF signal to the final orthogonal output signals at baseband frequency. The orthogonal LO signals are generated by a divider by 4 for the GSM850 and GSM900 band and by a divider by 2 for the GSM1800 and GSM1900 band.

The resulting in-phase and quadrature signals are fed into the baseband low pass filters providing sufficient suppression of blocking signals as well as of adjacent channel interferers and ensures the ADC's anti-aliasing requirements at 13MHz clock rate. A programmable gain stage for the correction of gain tolerances in thirteen 1dB steps (-6dB…+6dB) and the adaptation of the output signals to the baseband ADC's input dynamic range is implemented.

The IQ receiver signals are fed into the AD converters of the EGOLDlite and the differential baseband signals are digitalised separately for the I and Q path. On EGOLDlite both the digital and analogue baseband filters of the I/Q-interface are implemented. The analogue part of the baseband receive section comprises anti-aliasing pre-filters for in-phase and quadrature components and ΣΔ analogue-to-digital converters with approximately 12 bit (standard mode) and 14 bit (enhanced mode) resolution with 2 Vpp max differential input voltage. The complete ADC functionality comprises the ADC and the digital baseband receive filters.

The baseband receive filters are digital multi rate decimation low pass filters. They consist of several filter stages with decimations taking place as early as possible. The last filter stage is an adaptive switchable linear-phase FIR filter. Depending on the level of adjacent channel interference it selects a filter with appropriate frequency transfer characteristic for improved channel filtering. Furthermore, the filter coefficients of the last FIR filter stage are programmable for optimisation purposes.

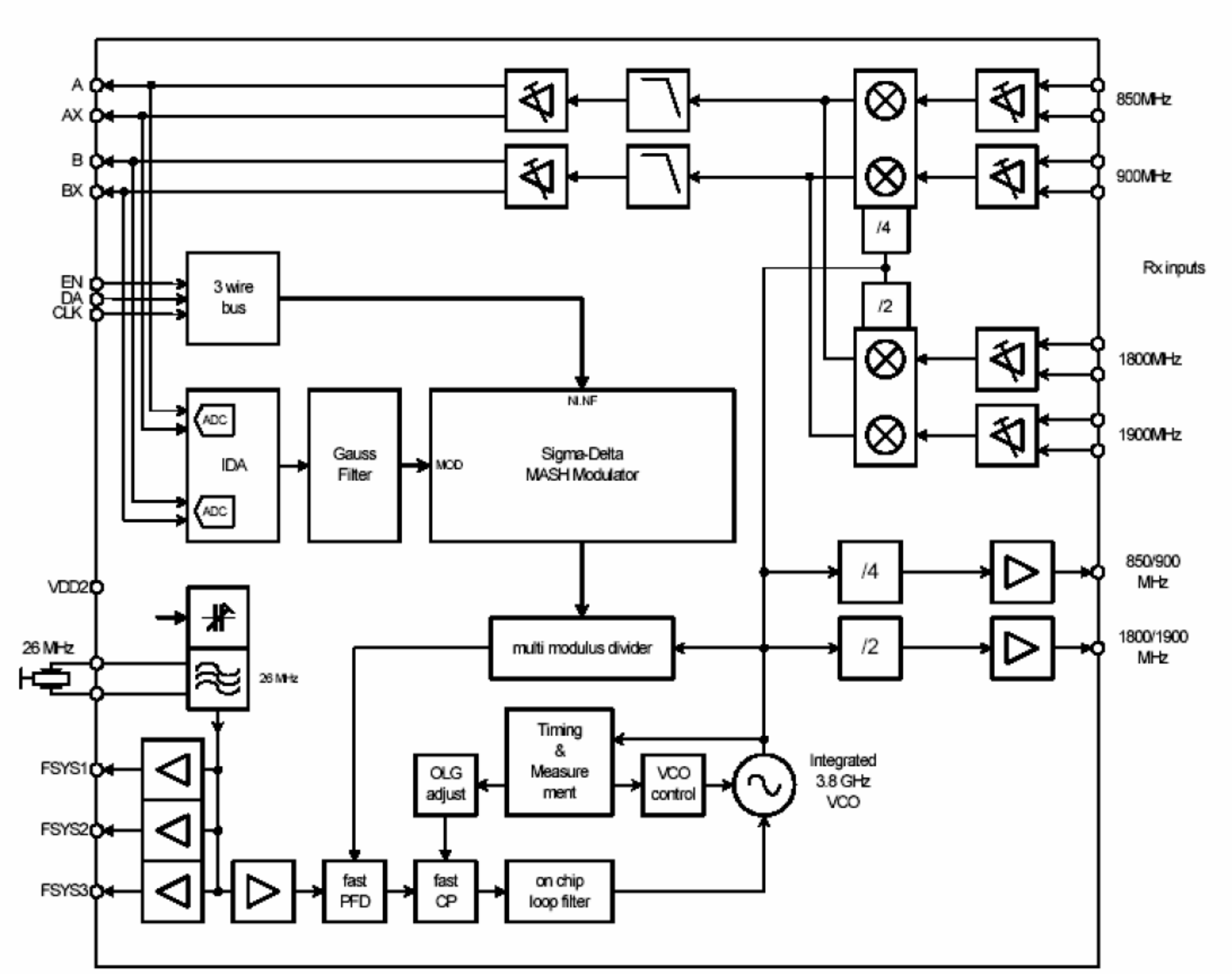
5.3.4 Transmitter (Sigma Delta)

The innovative part of the SMARTi SD2, the digital modulation principle, is as well established in the SMARTi SD2. Basis is the fact, that the GMSK modulation can be considered to be a phase modulation in its origin. This can be achieved by controlling the frequency of a VCO. There are various methods to do so. One of the smartest is to use a PLL for this application. The advantage of this method is a low effort in hardware and that a lot of unwanted spurs are not generated e.g. carrier- or sideband spurs. Therefore a calibration of the I/Q baseband signals to achieve sufficient sideband- and carrier suppression is not required any longer.

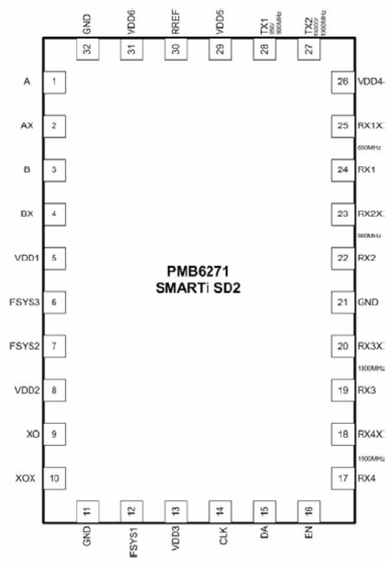
The I/Q signals are provided by the base band chipset with a 1.0V DC offset and amplitude of 0.94Vpp over balanced lines. The first step now is to convert the base band signal from analog to digital. After that the signal passes a digital gaussian filter and is fed to the mash modulator. This network is calculating the divider settings of the PLL. The VCO is oscillating from 3.42 GHz to 3.98 GHz. This is twice the frequency for the high band, so a division by 2 is necessary for DCS/PCS operation and a division by 4 for GSM 850/900 operation.

The output signal of the modulator is buffered with two different stages for GSM and DCS/PCS. The output stage is a single ended nominal 50Ω stage with about 3.5dBm output power, so no matching elements between SMARTi and PA are necessary.

Block diagram



Pinout



5.4 Antenna switch (electrical/mechanical)

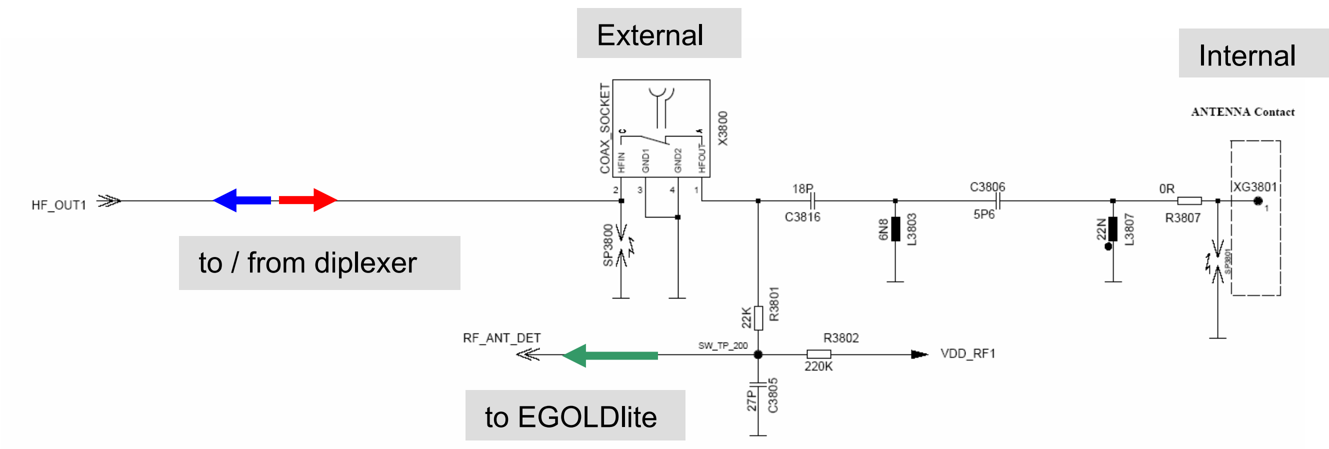
Internal/External <> Receiver/Transmitter
The AF51 mobile have two antenna switches.

a) The mechanical antenna switch for the differentiation between the internal and external antenna which is used only for RF adjustments on the board.

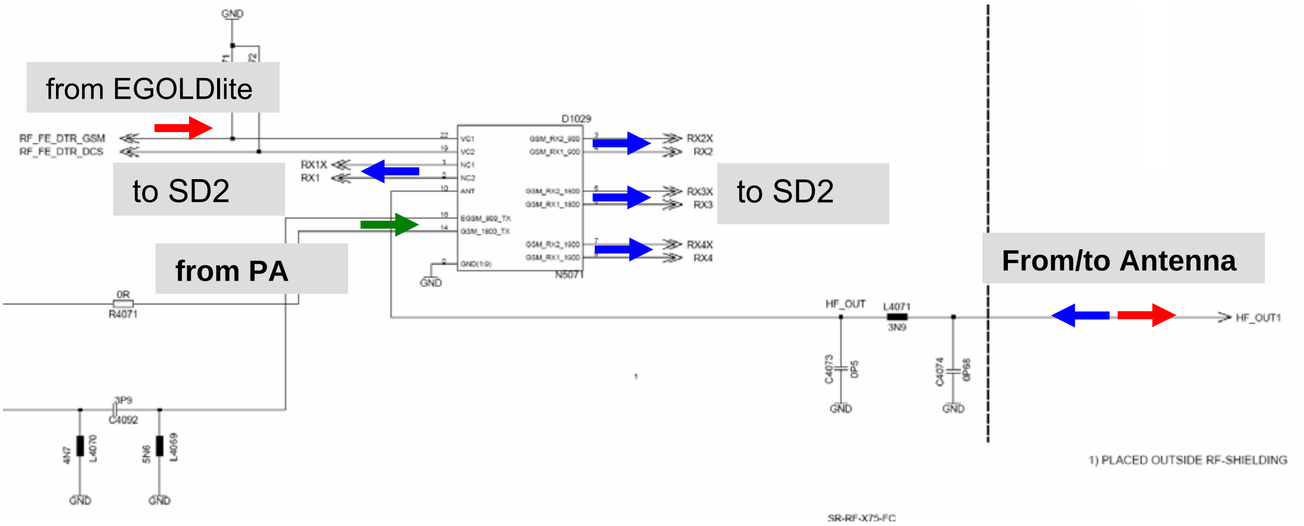
b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals.

To activate the correct tx pathes of this diplexer, the EGOLDlite signals RF_FE_DTR_GSM and RF_FE_DTR_DCS are required.

Internal/External antenna switch



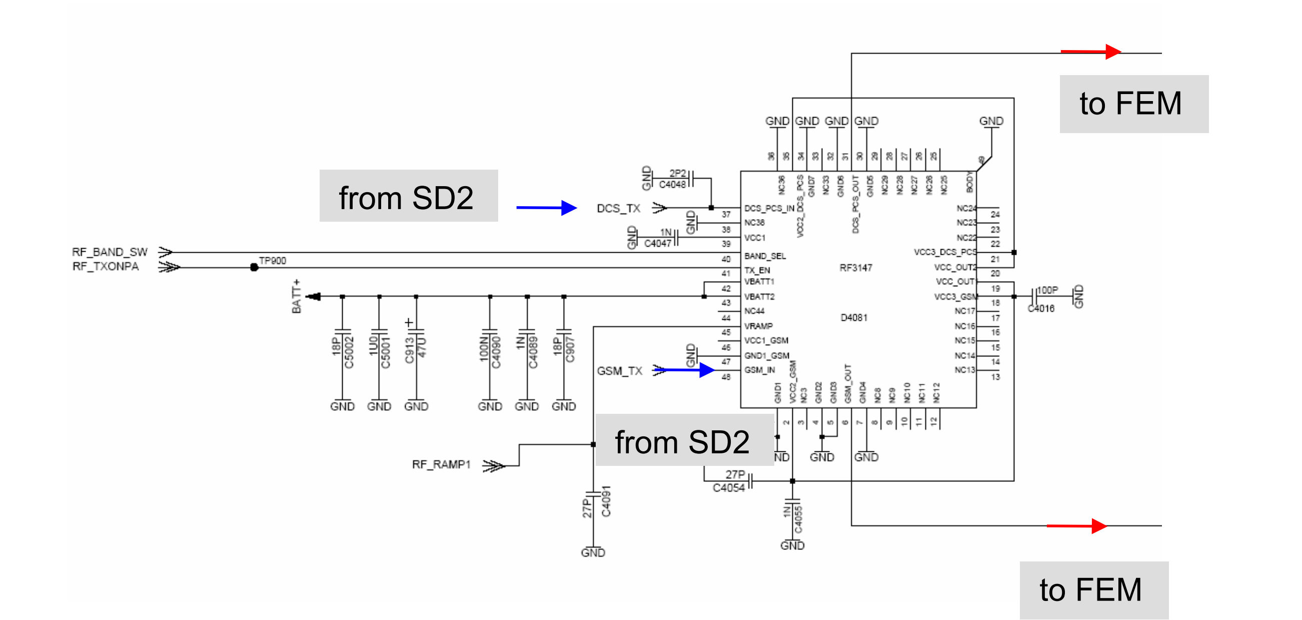
The electrical antenna switch



5.5 RF Micro Devices transmitter power amplifier RF3147

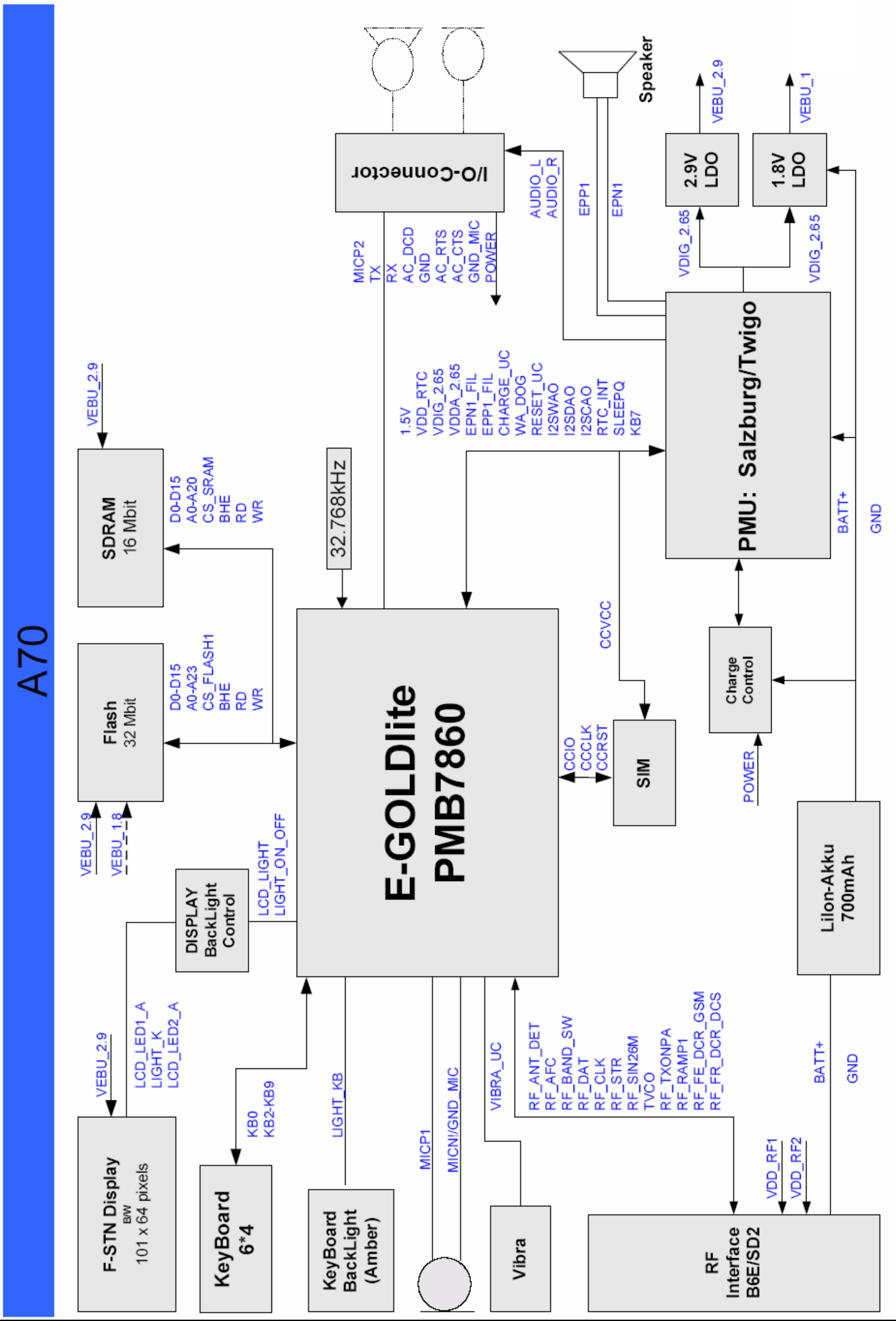
The power amplifier is a module from RF Micro Devices and matched to 50 Ω at all signal ports. It contains two separate 3-stage amplifier chains for GSM900 and GSM1800/GSM1900. It is possible to control the output-power of both bands via one VAPC-port. The appropriate amplifier chain is activated by a logic signal provided from the baseband. To ensure that the output power and burst timing fulfills the GSM-specification the power-controller is as well integrated in the module. The combination of antenna, antenna LPF, FEM and transmission lines will prevent the PA of critical mismatch phases. The power-controller itself is controlled by the PA-Ramp signal provided by the baseband.

The power-controller itself is controlled by the RF_RAMP1 signal provided by the EGOLDlite.



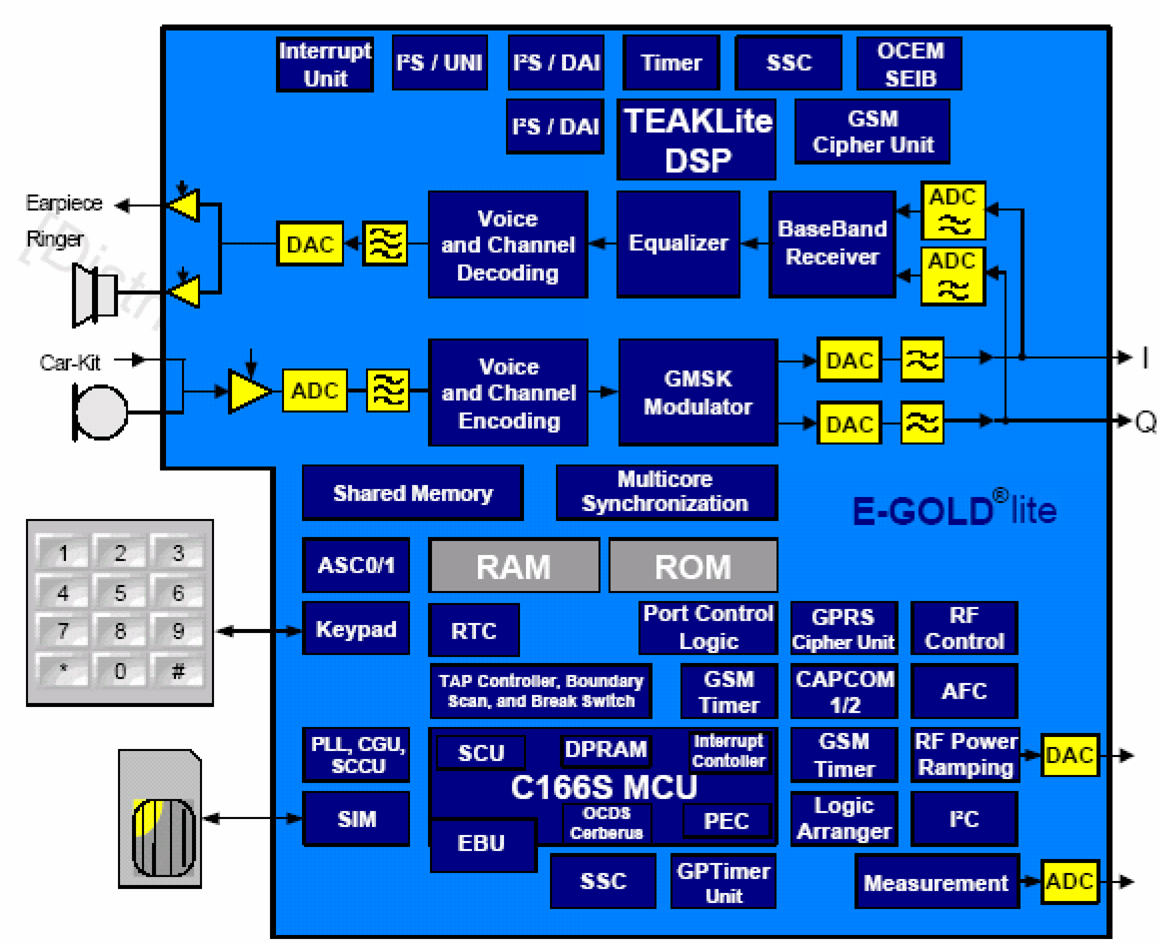
6 Logic / Control

6.1 Overview of Hardware Structure A70



6.2 EGOLDlite

6.2.1 Blockdiagram EGOLDlite



E-GOLDlite is designed as a single chip solution that integrates the digital and mixed signal portions of the baseband. It uses a leading 0.13 µm technology with a core voltage of 1.5 V. This allows and high performance mobile station with a large set of features at very low cost.
E-GOLDlite has a flexible set of interfaces that allows a wide choice of communication interfaces and supports a high multimedia data rate.

E-GOLDlite is powered by C166®S CPU and TEAKLite® DSP cores.

The E-GOLDlite is placed in a S-LF2BGA201 (a “flipchip” with 201 pins) with 0,5mm Ball-Pitch.

The E-GOLDlite is suited for mobile stations operating in the GSM850/900/1800/1900 bands.

In the receiver path the antenna input signal is converted to the base band, filtered, and amplified to target level by the RF transceiver chipset. The resulting differential I and Q baseband signals are fed into the E-GOLDlite. The A-to-D converter generates two 6.5 Mbit/s data streams. The decimation and narrowband channel filtering is done by a digital baseband filter in each path. The DSP performs:
1. The GMSK equalization of the received baseband signal.
2. Channel decoding, which is supported by an hardware accelerator.

The recovered digital speech data is fed into the speech decoder. The E-GOLDlite supports fullrate, halfrate, enhanced fullrate and adaptive multirate speech CODEC algorithms.

The generated voice signal passes through a digital voiceband filter. The resulting 4 Mbit/s data stream is D-to-A converted by a multi-bit-oversampling converter, postfiltered, and amplified by a programmable gain stage.

The output buffer can drive a handset ear-piece or an external audio amplifier.

In the transmit direction the microphone signal is fed into a programmable gain amplifier. The prefiltered and A-to-D converted voice signal forms a 2 Mbit/s data stream. The oversampled voice signal passes a digital decimation filter.

Speech and channel encoding (including voice activity detection (VAD) and discontinuous transmission (DTX)) as well as digital GMSK modulation is carried out by the E-GOLDlite.

The digital I and Q baseband components of the GMSK modulated signals (48-times oversampled with 13 MSamples/s) are D-to-A converted. The analog differential baseband signals are fed into the RF transceiver chipset.

The RF transceiver modulates the baseband signal to the desired frequency in the 850 MHz, 900 MHz, 1.8 GHz, and 1.9 GHz band using an I/Q modulator. The E-GOLDlite is able to support quad band applications.

Finally, an RF power module amplifies the RF transmit signal to the required power level. Using software, the E-GOLDlite controls the gain of the power amplifier by predefined ramping curves (16 words, 11 bits). The E-GOLDlite communicates with the RF chip set via a serial data interface.

The E-GOLDlite also includes battery charger support (various sensor connections for temperature, battery technology, voltage, etc.) and a ringer buffer.

For base band operation, the E-GOLDlite supports:
• High Speed Circuit Switched Data (HSCSD) class 4
• Packet-oriented data (GPRS) class 4 with a coding scheme from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.

If the E-GOLDlite is only used as a modem, then it supports:

- High Speed Circuit Switched Data (HSCSD) class 10
  Note: With a HSCSD class 10, there are a maximum of 4 received time slots and 2 transmitted time slots.
  The total maximum number of received and transmitted time slots is 5.

- Packet-oriented data (GPRS) class 10 with a coding scheme from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.
  Note: With a GPRS class 10, there are a maximum of 4 received time slots and 2 transmitted time slots.
  The total maximum number of received and transmitted time slots is 5.

The E-GOLDlite can support Class B operation. The mobile phone can be attached to both GPRS and GSM services, using one service at a time. During a GPRS connection Class B enables either:

- Making or receiving a voice call
- Sending or receiving an SMS.

During voice calls or SMS, GPRS services are suspended and then resumed automatically after the call or SMS session has ended.

E-GOLDlite is made with the Infineon C11N process using the High Voltage Threshold (HVT) and 5 Metal Layer (5LM).

The C11N process is a 0.13 µm technology. It is used for the logic, SRAM, mixed signal, and mixed voltage Input/Output applications.

C166S MCU

The C166S is a 16-bit CMOS (Complementary Metal Oxide Silicon) microcontroller. It contains a CPU (Central Processing Unit) core (the MCU) and a set of peripherals.

The architecture of the MCU combines both RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) architecture.

- High Performance 16-Bit MCU with a four-stage pipeline:
  - – 38 ns minimum instruction cycle time with most instructions executed in 1 cycle (2 clock ticks)
  - – 192 ns multiplication (16-bit x 16-bit), 384 ns division (32-bit/16-bit)
  - – Parallel use of multiple high bandwidth internal data buses
  - – Register based design with multiple variable register banks
    - – Single cycle context switching support
  - – 16 MBytes linear address space for code and data (von Neumann architecture)
  - – System stack cache support with automatic stack overflow/underflow detection.
- Control Oriented Instruction Set with High Efficiency:
  - – Bit, byte, and word data types
  - – Flexible and efficient addressing modes for high code density
  - – Enhanced boolean bit manipulation with direct addressing of 6 Kbits for peripheral
  - control and user defined flags
  - – Hardware traps to identify exception conditions during runtime
  - – HLL support for semaphore operations and efficient data access.
- External Bus Interface:
  - – Demultiplexed bus configurations
  - – Segmentation capability and chip select signal generation
  - – 8-bit or 16-bit data bus
  - – Bus cycle characteristics selectable for five programmable address areas.
- 16-Priority-Level Interrupt System:
  - – Up to 112 interrupt nodes with separate interrupt vectors
  - – 16 priority levels and 8 group levels.
- 16-Channel Peripheral Event Controller (PEC):
  - – Interrupt driven single cycle data transfer
  - – Transfer count option (standard MCU interrupt after programmable number of PEC transfers)
  - – Long Transfer Counter
  - – Channel Linking
  - – Eliminates overhead for saving and restoring system state for interrupt requests.

- DPRAM:
  - – Internal 16-bit dual port RAM with a 1K x 16-bit size.
- SCU (System Control Unit):
  - – Handles the boot and sleep mode of the core
  - – Provides a watchdog timer.

The architecture of the C166S combines the advantages of both RISC (Reduced Instruction Set Computing) and CISC (Complex Instruction Set Computing) processors in a well-balanced way. C166S based derivatives not only integrate a powerful MCU (Central Processing Unit) core and a set of peripheral units into one chip, but also connects the units in a very efficient way. One of the four buses used concurrently on the C166S is the Internal Bus Interface, an internal representation of the external bus interface. This bus provides a standardized method of integrating application-specific
peripherals to produce derivatives of the standard C166S.

The Principle Elements of a C166S Based System

- MCU block including the configurable Interrupt/PEC controller and debug and break logic
- Configurable dual port RAM
- Configurable Interrupt/PEC controller
- All interfaces for system (on chip) integration, including X-Bus, PD peripheral bus, Local Memory bus (for ROM or SRAM).

The C166 architecture allows instruction execution and data access from all memory locations. This includes X-Bus, local memory bus, dual port and external memories.

All four bus Interfaces of the MCU (X-Bus, LM Bus, RAM Bus and PD Bus) are operated on at the same time by the MCU.

<u>TEAKLite:</u>

The TEAKLite core has 16-bit data and 16-bit program memory accesses, a high performance fixed-point DSP core, and low power consumption.

The core consists of a high performance processing unit including a full featured bit-manipulation unit, RAM and ROM addressing units, and program control logic. The core has an improved set of DSP and general microprocessor functions to meet application requirements. The programming model and instruction set are optimized for generation of efficient and compact code.

The Computation Unit consists of a 16 by 16 multiplier unit with a 32-bit product and a 36-bit ALU with two accumulator registers A0 and A1.

The Bit Manipulation Unit consists of a full 36-bit barrel shifter, an exponent unit, a bit-field operation unit, two 36-bit accumulator registers B0 and B1, and a shift value register.

The Data Address Arithmetic Unit performs all the address storage and address calculation necessary for accessing the data and program memories. It also supports a software stack pointer, loop counter, and min/max operations.

The key features of TEAKlite core are as follows:

- 16-bit fixed-point DSP core
- 16 x 16-bit 2's complement parallel multiplier with a 32-bit product
- Single cycle multiply-accumulate instructions
- 36-bit ALU
- 36-bit left/right barrel shifter
- Four 36-bit accumulators
- Software stack residing in the data RAM
- User-defined registers off-core
- Three high-active interrupt input lines INT0, INT1, and INT2
- Automatic context switching by interrupts
- Up to 16-bit Bit Field Operations (BFO)
- Three modes for power saving features: Operational, Idle, and Sleep.
- The maximum Frequency is 104 MHz. The TEAKlite core clock is scalable to lower frequencies.

In the DSP Firmware are implemented the following functions:

The High Speed Circuit Switched Data (HSCSD) class 4 is supported.
The packet-oriented data (GPRS) class 4 is supported with a coding schemes from 1 to 4. It provides fixed, dynamic and extended dynamic modes.

If the E-GOLDlite is used as a modem, the HSCSD and GPRS class 10 is supported. The packet-oriented data (GPRS) class 10 is supported with a coding schemes from 1 to 4. It provides fixed, dynamic, and extended dynamic modes.

<u>Synchronisation and Measurements</u>

- Scanning of channels (measurement of the field strengths of neighboring base stations)
- Detection and evaluation of Frequency Correction Bursts.

<u>Equalization</u>

There is equalization of GMSK Normal Bursts and Synchronization Bursts with bit-by-bit soft output.

<u>Channel Coder/Decoder</u>

There are Channel Coders/Decoders for 2.4kbits/s, 4.8kbits/s, 9.6kbits/s, and 14.4kbits/s.

Speech
- A Speech Coder-Decoder: FR, EFR, AMR Narrow Band, or HR.
- Discontinuous transmission (DTX)
- Voice activity detection (VAD)
- Comfort noise generation (CNG).

Voiceband
- Generation of tones and side-tones
- Ringer tone generation
- Echo Cancellation (handsfree) with noise reduction

Also the functionality and the internal and external interfaces of the Audio Scheduler is implemented in DSP firmware of E-GOLDlite.

Real Time Clock (integrated in the E-GOLDlite):
The real time clock (degree of accuracy 150ppm) is powered via a seperate voltage regulator inside the PMU. Via a capacitor, data is kept in the internal RAM during a battery change for at least 30 seconds. An alarm function is also integrated with which it is possible to switch the phone on and off.

6.3 SRAM

Memory for volatile data

Memory Size:	A70 - 16 Mbit
Data Bus:	16Bit

6.4 FLASH

Memory Size:	A70 - 32 Mbit (4Mbyte)
Data Bus:	16 Bit

6.5 SIM

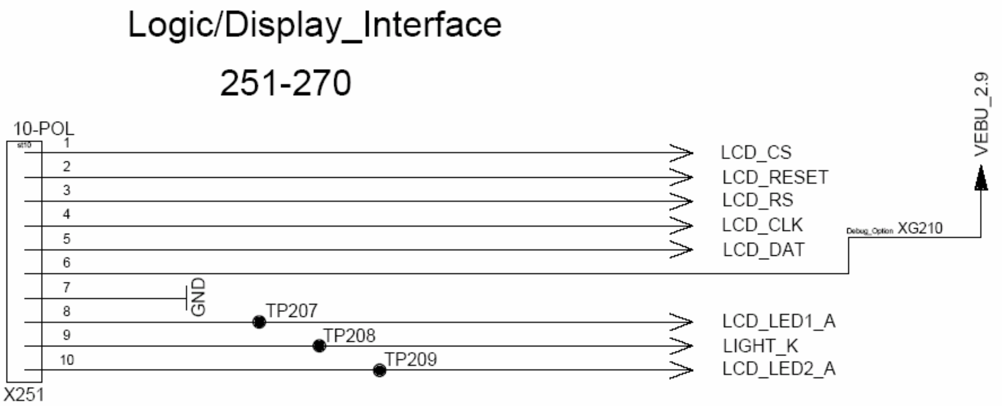
SIM cards with supply voltages of 1.8V and 3V are supported.

6.6 Vibration Motor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts.

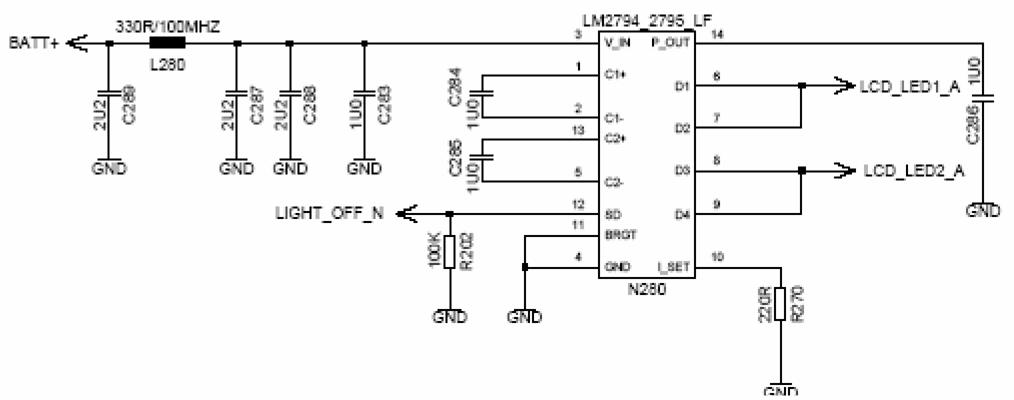
6.7 Display Modules

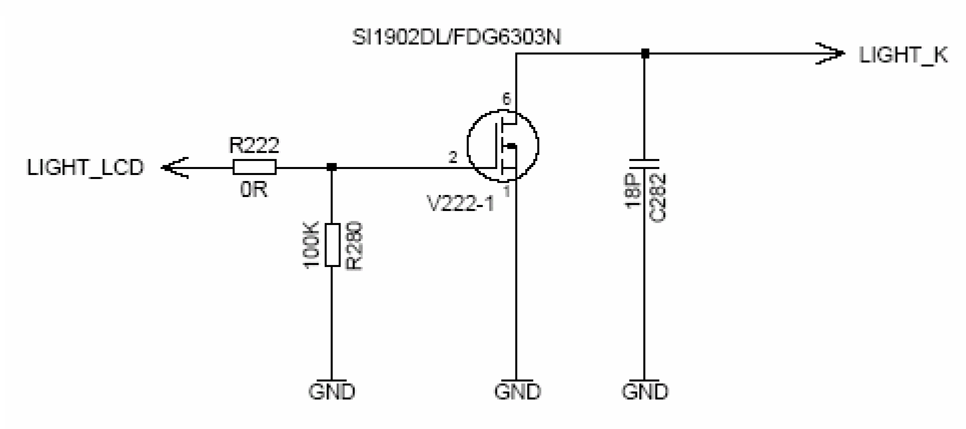
The A70 display has a resolution of 101x64 pixels b/w. It contains a passive addressed F-STN panel. The colour depth is switch-selectable by software. It contains a passive addressed STN panel where the colours are generated by colour filter (C-STN, Colour-Super Twisted Nematic). Different sources are used for the displays. The modules use different LCD-controllers. In order to guarantee a very efficient illumination the Amber LEDs are mounted on a PCB on the module. In addition, all passive components necessary to drive an LCD are assembled on the module PCB. Further, the hardware coding is also implemented on the module PCB. Thus, the only interconnections to the Siemens PCB are the data lines and the power supply lines of the controller and the amber LEDs. The interface is realised by a spring connector with 10 interconnections, which is assembled on the Siemens PCB.



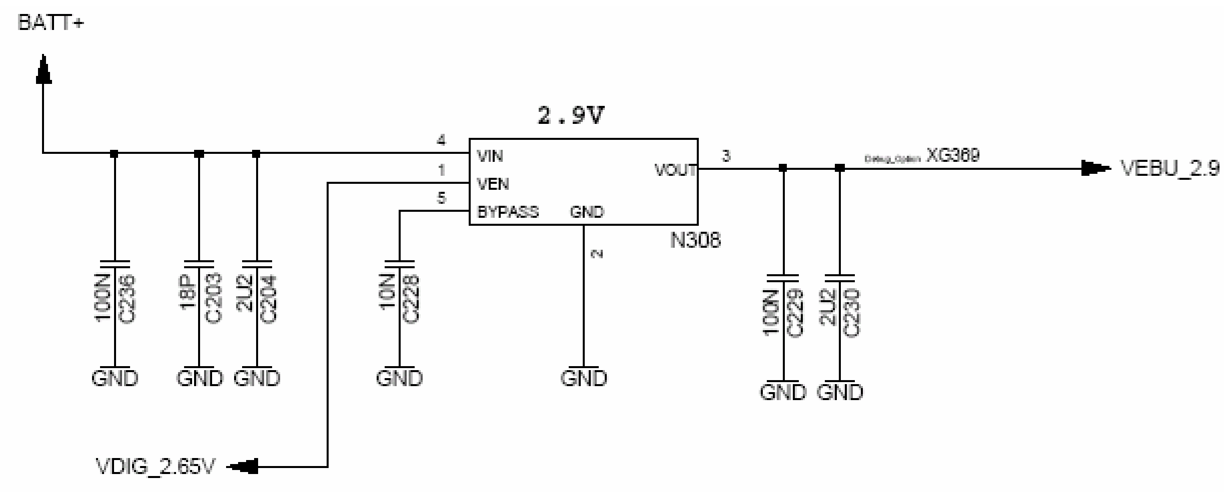
Pin	Name	Remarks
1	LCD_CS	Chip select
2	LCD_RESET	Reset
3	LCD_RS	Register select
4	LCD_CLK	Clock
5	LCD_DAT	Data line
6	2.9V	Power supply display controller
7	GND	GND
8	LCD_LED2_A	Power supply display led 2
9	LIGHT_K	Switched GND for display led 1 and led 2
10	LCD_LED1_A	Power supply display led 1

Required voltage for the display illumination is LCD_LED1_A and LCD_LED2_A.
The voltage regulator N280 with a nominal output voltage of 2.8V is used. With the signal LIGHT_LCD (P1) the illumination for the display is controlled.



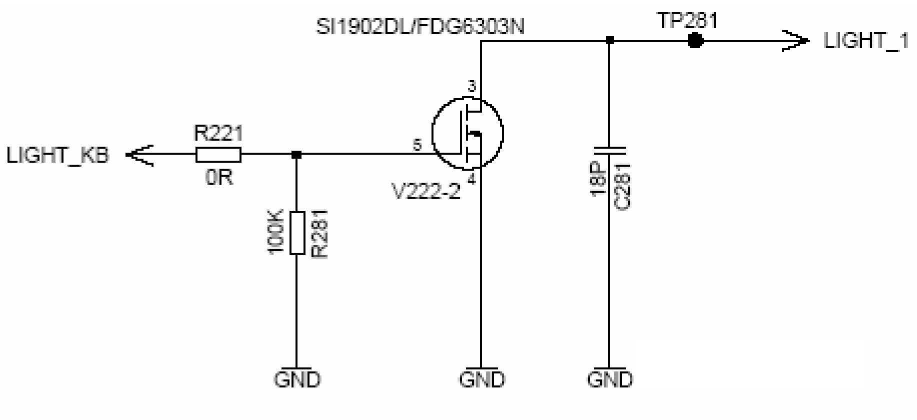


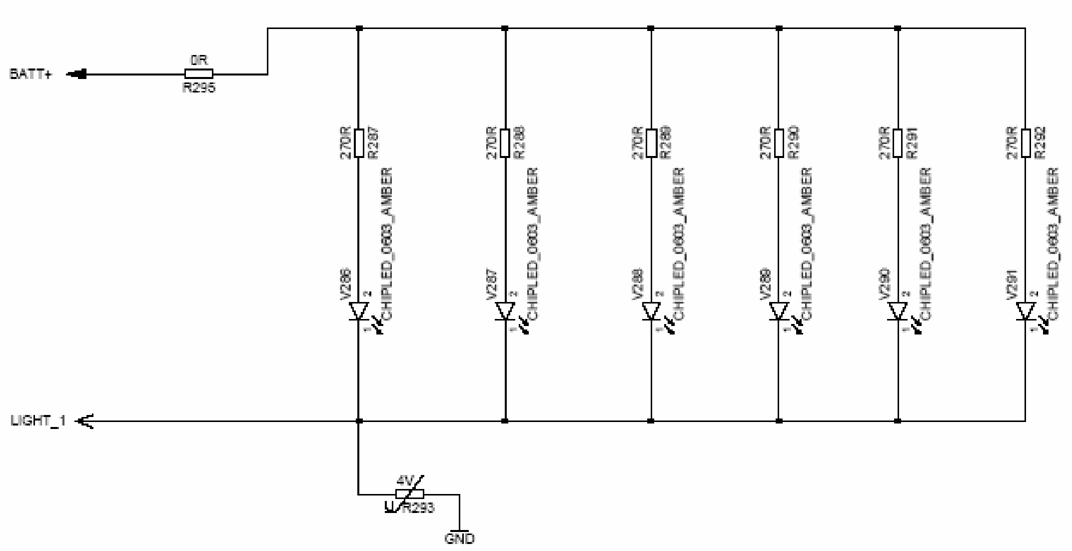
Required voltage for the display controller VEBU_2.9V.
The voltage regulator N308 with a nominal output voltage of 2.9V is used



6.8 Illumination – Keyboard

The LED´s are mounted on the upper side of the PCB. The illumination of the keypad will be done via high-brightness LEDs (colour: amber, type: top-shooter, driven by 6 mA / LED). The light is switched via switches inside the EGOLDlite. With the signal LIGHT_KB (R5) the illumination for the keyboard is controlled.





7 Acoustic

The speaker module is designed to provide good performance for mobile handsfree and sound ringer. The speaker module is a system which has a closed front volume with sound-outlets towards the ear of the user. The speaker is partly hidden behind the display to save length of the phone. The back volume of speaker module is using the unused air between the antenna and the PCB. The speaker module is connected to the SAR-frame and contacted via two bending springs to the PCB. For avoiding any interference between antenna and earpiece, there is an antenna reference plate soldered behind the speaker at the PCB. In ringer mode acoustic shock is avoided by using ramping of the ringer level.

The microphone is built in the Mounting Frame Lower Part and is mechanically fixed with a rubber seal (gasket). The contact on the PCB is realised via spiral springs, which are integrated in the gasket. Because of usage of Unidirectional Microphone, the gasket has a front- and a back sound-inlet hole. The front sound-inlet is acoustically tighten connected with a sound-inlet at the rear-side of the mounting frame lower part. The back sound-inlet is acoustically tighten connected with a sound-inlet at the bottom-side of the mounting frame lower part. The gasket of the microphone has a asymmetrical shape in order to provide non-rotating, guaranteed covering of the sound-inlets of mounting frame lower part to the corresponding sound-inlets at microphone gasket.

The buzzer and the keypad clicks will be realized over the earpiece.

The standard sounds will be generated by the EGOLDlite, the advanced sounds will be generated via firmware running on the DSP.

8 Power Supply, Battery and Charging

All the important functions for the power supply of the phone are carried out by the power supply ASIC.
The POWER-pin of the I/O-Connector is for charging the battery with an external power supply.

8.1 Power Supply ASIC

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- Voltage regulator
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I2C interface)
- Bandgap reference
- Audio multiplexer
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I2S Interface

Power Supply Operating modes:

The ASIC can be used in different operating modes:

Mode	Pin Requirements	Description
Power down mode with minimum activity	ON/OFF ON/OFF2 VDD_CHARGE	In power down mode the current consumption of the ASIC is very low. The inputs for switch on conditions (Pin ON/OFF, ON/OFF2,VDD_CHARGE), the LPREG, Bandgap reference, and the POR cells are active. All other blocks are switched off, so the battery is not discharged. This state is called “phone off.
Start Up Mode	ON_OFF ON_OFF2	Start Up Mode can be initiated by ON_OFF or ON_OFF2. In this mode a sequential start-up of references (this includes the reference buffer and the biasing cell), oscillator., voltage supervision and regulators is controlled by digital part. In failure case (undervoltage, overvoltage or time out of the µC reaction)., the ASIC is shut down.
Full operating mode	VDD_CHARGE CHARGE_UC	All blocks are active. Trickle charge is switched off. The blocks fast charge and charge monitor can be active only in this mode. These modes will be activated with VDD_CHARGE or CHARGE_UC. The name of this mode is “phone on” or “active mode”. The border between the startup phase and the active mode is the rising edge of the RESETN signal. This will allow the uC to start working.

Mode	Pin Requirements	Description
Active Mode (submode of Full operating mode)		In this mode, the uC controls the charging block and most of the failure cases. The ASIC can be controlled by the TWI interface, interrupts can be sent by the ASIC. Further, the temperature and the voltages are supervised (in case of failure, the uC will be informed). In case of watchdog failure, overvoltage or power on reset, the ASIC will be switched off immediately. The mono and stereo audio block can be switched on in active mode.
Sleep Mode with special low current operating mode for the LDOs (submode of Full operating mode)	SLEEP1_N TC_ON CHARGE_uC	A low level at the pin SLEEP1_N will switch the phone from the mode "PHONE ON" to sleep mode. This mode can be activated out of the active mode. In sleep mode trickle charge (TC_ON), fast charge (CHARGE_UC), supply overvoltage detection, supply undervoltage detection, audio function are switched off. LDO undervoltage detection, clock and all reference voltages are active. LDOs are working in low current mode. The possibility to supply the ASIC from VDD_CHARGE with the internal LDO is switched off. Only the battery can be used for supply. This mode is called "phone stand-by".
Trickle charge mode to be able to support charging of the battery	VDD_CHARGE EXT_PWR	In case of a rising edge at VDD_CHARGE the ASIC goes from power down to interim mode. In this mode, the oscillator and the reference are started. The fuses are read in. If the voltage is high enough (after a delay time of 1 ms to filter a ringing), the signal EXT_PWR is going to H and the power up continues. The ASIC shuts off if the voltage is below threshold. In Trickle Charge Mode, first the charge unit starts and charges the battery in case of undervoltage. After reaching this threshold voltage or if the battery has enough voltage from the beginning, a start up similar to the regular startup mode is initiated. In case of voltage drop under battery threshold, the first trickle charging can be started again until the Active Mode is entered. In this case, the internal VDDREF regulator, the reference generator and oscillator are started and the ASIC is supplied by VDDREF. If any failure is detected, the ASIC is switched off.

Power Supply Functions:

Functions	Pin Requirements	Implementation/Sequence
Switching on the mobile phone	ON_OFF, ON_OFF2, VDD_CHARGE	There are 3 different possibilities to switch on the phone by external pins: - VDD_CHARGE with rising edge after POR or high level at end of POR signal - ON/OFF with falling edge - ON/OFF2 with rising edge In order to guarantee a defined start-up behaviour of the external components, a sequential power up is used and the correct start up of these blocks is supervised. In active mode, a continuous signal at watchdog is needed to keep the system running. If the signals fails, the ASIC will switch to power down mode. It must be guaranteed that each start-up condition does not interfere and block the other possible startup signals. In case of failure during start-up, the device will go back to power down mode. To guarantee that VDDCHARGE is always sensed we must be able to detect whether the VDDCHARGE will have a rising edge during POR (this can happen in case of an empty battery). Therefore this signal is sensed as level sensitive at the end of POR and edge sensitive after POR signal.
Watchdog monitoring	WDOG	As soon as the first WDOG pin rising is detected during the TE4 timer, the device start the watchdog monitoring procedure. Standard switch off of the phone is the watchdog. The first edge of watchdog is rising. If a falling edge is detected as the first transient the device will go to power down mode again and the whole phone is switched off. Rising and falling edges must be detected alternated. With any edge on WDOG pin a counter will be loaded. The next - compared to the previous edge - inverted edge must occur between end of T1, and end of T2. If the signal occurs before end of T1 or is not detected until end of T2, the device will go to power down mode immediately after the violation of the watchdog criteria occurs. T1 min. 0,327s/ typ. 0,360s/ max. 0,400s T2 min. 2,600s/ typ. 2,860s/ max. 3,178s
Power-On-Reset (POR)	RESET_N RESET2_N	To guarantee a correct start-up of the ASIC, a power on reset is needed at first power supply ramping. Therefore a static/dynamic power on reset circuit is added, which creates a reset each time the power supply is connected. After POR the ASIC starts up the reference and the oscillator, read in the fuse content and goes back to power down mode. If the power supply will drop under the POR threshold V_{th,POR_L} a synchronous reset is done and the ASIC will go to power down mode independently of the previous operating mode. V_{th,POR_L} = min. 2.38/ typ. 2.43/ max. 2.48V

Functions	Pin Requirements	Implementation/Sequence
Voltage Supply Logics	REG1 (2.65V)	The linear controller is designed for 2.65V(±2%) and a maximum load current of 140 mA. Voltage and current for the external Logic is supplied from the internal 2.65V logic regulator. The operating voltage VREG1 is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference
Voltage Supply Logics	REG2 (1,5V)	The linear controller is designed for 1.5V (±2%) and a maximum load current of 300 mA. The output voltage can be adjusted to four different values with TWI register by the µC. The selectable values are 1.5(default), 1.82, 1.92 and 2.0V. The REG2 supplies the Baseband Processor.
Voltage Supply Logics	REG3 (2.65V)	The linear controller is designed for 2.65V(±3%) and a maximum load current of 140 mA. It will consist basically of an internal operation amplifier, an integrated p-channel output transistor as well as a capacitor (C = 2.2µF) for stabilising the voltage. The required reference voltage for the regulating circuit will be generated internally via a band gap. The negative feedback of the regulating circuit shall be done via chip-internal resistances.
Voltage Supply RF	VREGRF1, SLEEP1_N, SLEEP2_N, POWER_ON	The linear controller is designed for 2.755V (±2%) and a maximum load current of 150 mA. The output voltage can be adjusted to three different values with TWI register by the µC. The selectable values are 2.755V(default), 2.54V, and 2.85V. Voltage and current for RF-VCO and Transceiver is supplied from the internal 2.755V LDO. The operating voltage RF1LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed. RF1LDO is controlled by SLEEP1_N and SLEEP2_N. If one of them is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF1LDO can only be enabled by TWI bit. In external mode, RF1LDO can only be enabled by SLEEP1_N or SLEEP2_N. RF1LDO is released with rising edge of POWER_ON signal.
Voltage Supply RF	VREGRF2, RF_EN, RESET_N	The linear controller is designed for 1.53V (±2%) and a maximum load current of 180 mA. The output voltage can be adjusted to three different values with TWI register by the µC. The selectable values are 1.53V(default), 2.70V, and 2.85V. Voltage and current for RF-VCO and Transceiver is supplied from the internal 1.53V LDO. The operating voltage RF2LDO is kept constant up to the maximum rated load current. A reference voltage for the regulator circuit is generated from a bandgap reference. A low noise must be guaranteed. RF2LDO is controlled by RF_EN. If it is set to high, the regulator is enabled. The control method can be modified by TWI interface between external and internal control mode. If internal control mode is set, RF2LDO can only be enabled by TWI bit. In external mode, RF2LDO can only be enabled by RF_EN. RF2LDO is released with rising edge of RESET_N signal.

Functions	Pin Requirements	Implementation/Sequence
Voltage Supply Audio	VREGA	The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 190 mA. VDDA is used for the whole stereo analog supply. The DAC digital (VDDDAC), Low Noise Bandgap, Mono- and Stereoamplifier supplies are connected to VREGA or VBAT or an external LDO at 2.9V +/-5%. The AUDIO performances are guaranteed only, if the VREGA supplies all the stereo path. VREGA is controlled with TWI registers directly by the µC.
Voltage Supply RTC	VLPREG	The linear controller is designed for 2.00V(min. 1.9V, max. 2.1V) and a maximum load current of 1 mA. The output voltage can be adjusted to four different values with TWI register by the µC. The selectable values are 2.00(default), 1.82, 1.92 and 2.07V. LP-LDO is always working and will switch of only with POR signal.
Voltage Supply SIM	VREGSIM	The linear controller is designed for 2.9V(min. 2.84V, max. 2.96V) and a maximum load current of 60 mA. The output voltage can be adjusted to a different value with TWI register by the µC to 1.8V(min. 1.76V, max. 1.84V). This regulator can be activated by TWI register, but only in active mode. If the regulator is in power down, the output is pulled down by a transistor to avoid electrostatic charging of VREGSIM.
Charge Support	CHARGE_UC, CHARGE, VDDCHARGE, AVDD, SENSE_IN, TBAT	A charge support will be integrated for controlling the battery charge function. It consists basically of a temperature sensor, an external charge FET, an integrated High-side driver for the external FET with an external resistor between the source and the gate of the charge FET. In the case of a rising edge at the CHARGE_UP the power source will be switched on. In this way the charge FET becomes conducting, provided that the integrated temperature comparator does not give the signal for extreme temperature and that no overvoltage is present at the VDD. In the case of falling slope at the CHARGE_UP, the current source is switched off and the pull-up resistor will make sure that the charge FET is blocked after a finite time. Temperature switchoff becomes effective at approx. T>60°C.
Voltage supervision		The levels of regulator REG1, REG2, REGA, SIM_LDO, and also the supply voltage VBAT are supervised with comparators.
Supervision of REG1 and REG2	REG1 REG2	In active mode the regulators are supervised permanently. If the voltage is under the threshold, the pin RESET_N stay Low and the ASIC go back to the power down mode. If the voltage is longer than Tmin under threshold voltage, the RESET_N is going to Low (Missing Watchdog signal -> phone switched off). The level of regulator REG1 and REG2 will be supervised permanently. If the voltage doesn't reach the threshold value at switch on, the RESET_N pin will stay low and the ASIC will go back to power down mode. The voltages are sensed continuously and digitally filtered with a time constant Tmin. If the regulator voltage is under threshold longer than Tmin, the RESET_N signal change to low and the uC will go to RESET condition (Missing Watchdog signal -> phone switched off).

Functions	Pin Requirements	Implementation/Sequence
Powersupply supervision	VDD	If the battery voltage VDD exceeds VDD_high everything is switched off immediately within 1µs. Only the pullup circuitry for the external charge PMOS are active and will discharge the gate of the external PMOS
VDDA supervision	VDDA	To provide a short circuit protection at output of VDDA and output of stereo buffer a voltage supervision is implemented. If the VDDA output is less then this threshold, the VDDA will be switched off for 128ms. After this time the VDDA will be started again. The VDDA supervision starts 60ms after startup of VDDA.
Battery temperature supervision		Charging is stopped, when overtemperatur occurs. Within 128ms, 3 values are measured. When these 3 values are identical status can be changed. The supervision is active in fast charge or trickle charge mode. Voltage on pin TBAT becomes smaller when temperature increases. If Vbat < (Vref_exe - Vhyst) charging is disabled. Only when Vtbatt > Vref_exe charging is enabled again.
Device temperature supervision		To protect the ASIC, the temperature is supervised. The temperature is polled every 128ms and is filtered as in battery temperature supervision. If overtemperatur is detected, a bit in the STATUS register is set and an interrupt is generated. Monitoring is started only in active mode.
Analog switch Outport		The level can be defined by the bit out_port_high of the TWI register. The high level can be derived of VREG2 or VREG3. Additional a pulldown transistor is connected to this node.
TWI Interface	TWI_CLK, TWI_DATA, TWI_INT	The TWI interface is an I2C compatible 2-wire interface with an additional interrrupt pin to inform the µC about special conditions. The interface can handele clock rates up to 400 kHz. The device adress is 010001B (31H)
Audio mode functions		Four audio amplifiers are integrated to support these modes: 1. Supply the speaker in the phone with audio signals including the possibility of handsfree and antipop switch on and off. This is the AUDIO MONO MODE. 2. Supply the speaker in the phone with ringing signal (RINGER MODE) 3. Transfer a key click, generated in digital part to the speaker. (KEY-CLICK FUNCTION) 4. Supply of stereo head set with stereo signal with short circuit protection. This is called the AUDIO STEREO MODE. These different modes with gain and multiplexing can be controlled via TWI. Also the output can be switched to TRI-STATE via TWI interface.

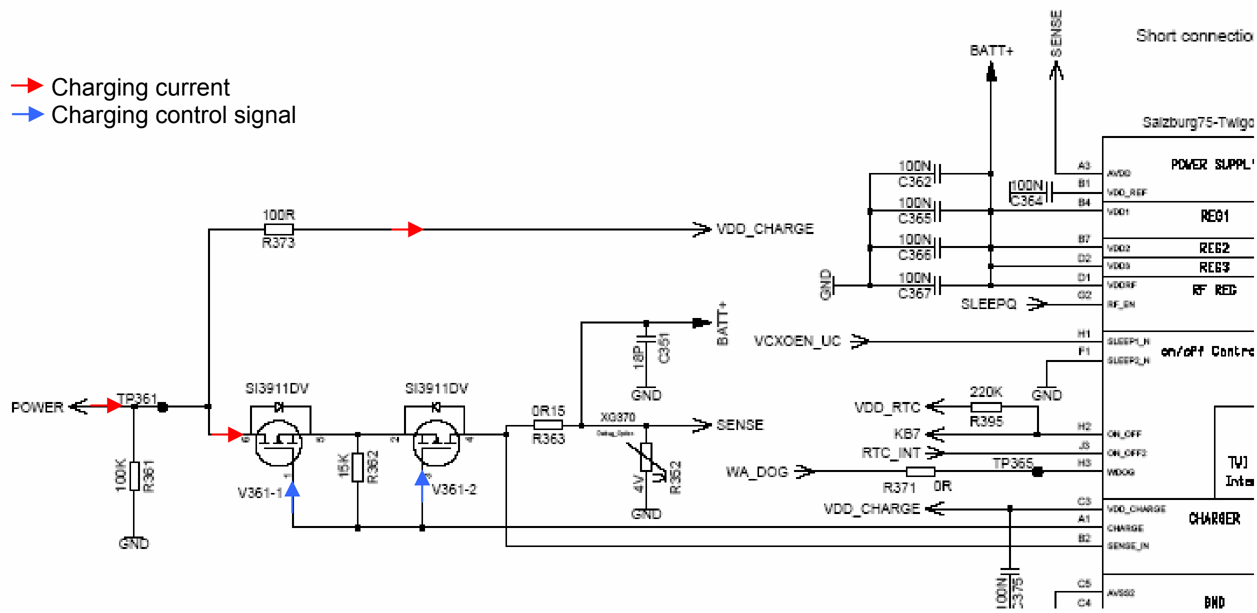
Functions	Pin Requirements	Implementation/Sequence
Audio Mono Mode	VREGA MONO1 MONO2 VREFEX_M	This mode is the main function of the amplifier. The two amplifiers are used as differential mono amplifier to drive the speaker in the phone as external load. This differential approach allows delivering an optimum of power to the speaker, also in low voltage mode. Both amplifier paths are inverting amplifiers with external AC coupling at the input to compensate offset failures. The gain can be adjusted with the TWI interface. The output stage of the amplifiers must be able to drive a low impedance load as a external speaker for the handsfree application. General parameters: Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB. The signals for the amplifier are connected via an audio multiplexer with 3 pairs of input signals.
Audio Stereo Mode	VDDSTEREO STEREO1 STEREO2 STEREOM	For stereo mode 2 single ended buffers are used. These buffers will be supplied by the additional regulator with 2.9 Volt to be more stable against the GSM ripple on the battery voltage. Also reference voltage for the buffers is generated by a high precision, low noise bandgap reference for better performance. An external capacitor is needed to filter this reference additionally. The gain steps for the programmable gain amplifier are identical with the mono amplifier. Nokeyclick and ringer needed for the stero part. Gain can be controlled with the TWI. The connected speaker has an impedance of typical 16 Ohm. To guarantee a ANTI-POP noise a digital startup is implemented. This will allow a soft start of the VMID and creates a “clean” audio band during the startup. For eliminating external coupling capacitors for the speaker, an additional amplifier creates virtual ground (for both speakers). Accordingly to this, the max current of the virtual ground has to be the double of the normal output amplifier. Due to the power amplifier offset a DC current appear in the headset. Gain can be adjusted for each channel separately in steps of 1.5dB in the range of 21dB to –54 dB and in steps of 3 dB in the range of –54dB to –75dB
Ringer function	RINGIN	In ringer mode the ringing signal is transferred via the amplifier to the speaker to eliminate the additional buzzer. The speaker is controlled with a rectangular signal RINGIN. Input signal is digital signal with variable frequency. Amplitude is adjusted by TWI register. For start-up a smaller time constant must be used to allow a fast switch on behaviour. Ringing function can be started at any time. If the audio is off, the start-up is done with RINGER time constant. If audio is starting with AUDIO start-up, the time constant is switched to RINGER mode, too. If the audio amplifier is already up and running, the RINGIN is connected to the amplifier and audio sigal is muted due to open multiplexer.

Functions	Pin Requirements	Implementation/Sequence
Key click function		Pushing a key of the phone can be combined with a key click. This function is also realized with the audio amplifier in pulsed mode. The ASIC creates a digital PWM signal. Frequency of the PWM signal is 3.5 kHz. The start-up is similar to the ringer function. If the audio is off, the start-up is done with KEYCLICK time constant. If audio is starting with AUDIO start-up, the time constant is switched to KEYCLICK mode, too. If the audio amplifier is already up and running, the KEYCLICK is connected to the amplifier and audio sigal is muted due to open multiplexer.
Audio Multiplex Matrix	AUDIOA1 AUDIOA2 AUDIOB1 AUDIOB2 AUDIOC1 AUDIOC2	Each of the three input sources should be switched to Mono and Stereo outputs. Furthermore a conversion can be done. Following sources: - Mono differential - Mono Single Ended (both channels parallel) - Stereo The DAC can be switched off for using the analog external inputs. This principle will allow to do each combination and have different modes for stereo and mono in parallel.
I2S Interface	CLO, WAO, DAO	The I2S Interface is a three wire connection that handels two timemultiplexed data channels. The three lines are the clock (CLO), the serial data line (DAO) and the word select line (WAO). The master I2S also generates the appropriate clock frequncy for CLO set to 32 times the sampling rate (FS)
Audio DAC	VDDDAC	For digital to analog conversion a 16 bit sigma delta converter is used. Digital input signal is delivered with a I2S interface. The I2S interface should be 16 bit format. To be able to work with allpossible operating modes, the sampling frequency can vary from 8kHz to 48kHz. The performance of the audio output signal must be guaranteed over the full range the human ear is able to hear. This means for FS=8kHz the noise at frequencies higher than FS/2 must be suppressed. This is done by DSP in a single ended 2nd order Low Pass filter. The clock for the I2S will be varied accordingly to the sampling frequency. Therefore a clock recovery based on CLO signal of the I2S can be implemented. This clock recovery must smooth any jitter of this clock to reduce the noise of the DAC.
PLL	VDDPLL PLLOUT	The PLL will have three frequency modes to produce a 32xCLO clock for the DSP and the DAC. The loop filter is realised with an external RC circuit. This PLL also contains a lock detector circuit.

8.2 Battery

As a standard battery a LiIon battery with a nominal capacity of 3,7 Volt/700mAh is used.

8.3 Charging Concept



8.3.1.1 Charging Concept

General

The battery is charged in the unit itself. The hardware and software is designed for LiIon with 4.2V technology.

Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging takes place in the background (the customer can see this via the "Charge" symbol in the display). During normal use the phone is being charged (restrictions: see below).

Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The EGOLDlite takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the POWER SUPPLY ASIC hardware can override/interrupt the charging in the case of over voltage of the battery (only for Manganese Chemistry Battery types e.g. NEC).

With the new slim Lumberg IO connector we lose the charger recognition via SB line. Now we measure the charge current inside the POWER SUPPLY ASIC with a current monitor.

The charging software is able to charge the battery with an input current within the range of 350-600mA. If the Charge-Fet is switched off, then no charging current will flow into the battery (exception is trickle charging, see below).

For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC. The NTC for the ambient temperature will be on the PCB (26 MHz part).

Measurement of Battery, Battery Type and Ambient Temperature
For the conversion of signals like battery voltage, battery type, temperature, EGOLDlite provides identical measurement interfaces. Measurement circuit is consisting of external sensing components and integrated analog multiplexers and switches. Through corresponding switch settings, the measured signal is passed to input of ADC. 12-bit conversion results are readout by µc and used for charging control.

Charging Characteristic of Lithium-Ion Cells
LiIon batteries are charged with a U/I characteristic, i.e. the charging current is regulated in relation to the battery voltage until a minimal charging current has been achieved. The maximum charging current is approx. 600mA, minimum about 100mA. The battery voltage may not exceed 4.2V ±50mV average. During the charging pulse current the voltage may reach 4.3V. The temperature range in which charging of the phone may be started ranges from 5...40°C, and the temperature at which charging takes place is from 0...45°C. Outside this range no charging takes place, the battery only supplies current.

Trickle Charging
The POWER SUPPLY ASIC is able to charge the battery at voltages below 3.2V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the POWER SUPPLY ASIC. The current level during trickle charge for voltages <2.8V is in a range of 20-50mA and in a range of 50-100mA for voltages up to 3.75V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the POWER SUPPLY ASIC will switch on the phone automatically and normal charging will be initiated by software (note the restrictions on this item as stated below).

Normal Charging
For battery voltages above 3.2 Volt and normal ambient temperature between 5 and 40°C the battery can be charged with a charge current up to 1C*. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the POWER SUPPLY ASIC. The level of charge current is limited/controlled by the accessory or charger.

Restrictions

- A battery which has completely run down can not be re-charged quickly because the battery voltage is less than 3.0V and the logic which implements the charge control cannot be operated at this low voltage level. In this case the battery is recharged via trickle-charging. However, the charging symbol cannot be shown in the display because at this time logic supply voltages are not operating. The charging time for this trickle-charging (until the battery can be fast-charged from then on) is in the range of 1 hour. If, within this time, the battery voltage exceeds 3.2V, then the PMU switches on the mobile and charging continues in the Charge-Only Mode. In some circumstances it can happen that after trickle-charging and the usually initiated switch-on procedure of the mobile, the supply voltage collapses so much that the mobile phone switches off again. In this case trickle charging starts again with a now raised threshold voltage of 3.75V instead of 3.2V, at maximum for 20 minutes. The PMU will retry switching on the phone up to 3 times (within 60 minutes overall).
- Charging the battery will not be fully supported in case of using old accessory (generation '45' or earlier). It is not recommended to use any cables that adapt "old" to "new" Lumberg connector. Using such adapters with Marlin will have at least the following impact:

1) half-sine wave chargers (e.g. P35 & home station) can not be used for trickle charging
2) normal charging might be aborted before the battery is fully charged
3) EMC compliance can not be guaranteed

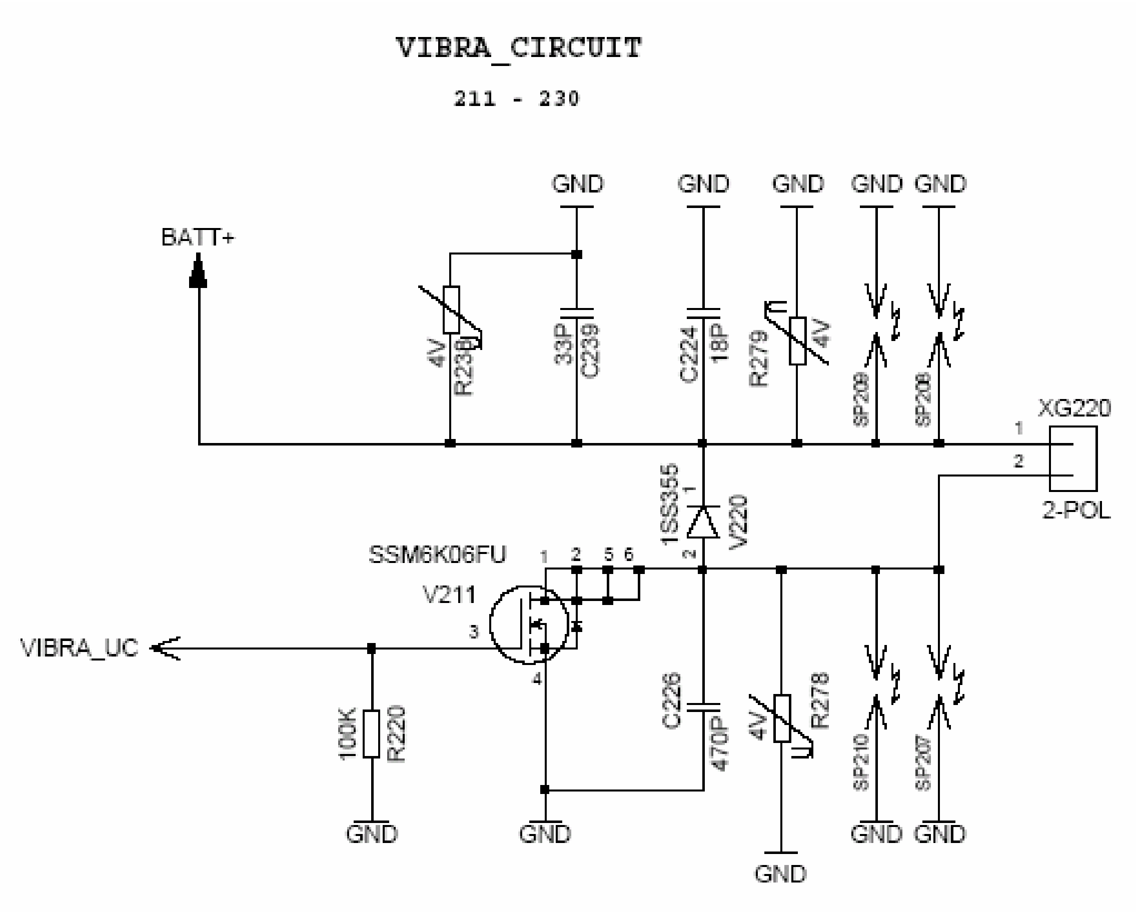
- A phone with a fully charged LiIon battery will not be charged immediately after switch-on. Any input current would cause an increase of the battery voltage above the maximum permissible value. As soon as the battery has been discharged to a level of about 95% (due to current consumption while use), it will be re-charged in normal charging mode.

- The phone cannot be operated without a battery.
- The phone will be destroyed if the battery is inserted with reversed polarity.
- The mobile phone might be destroyed by connecting an unsuitable charger.

In case the transistor fails the ASIC will be destroyed. In the case of voltages lower than 15V and an improper current limitation the battery might be permanently damaged. A protection against grossly negligent use by the customer (e.g. direct connection of the charge contact to the electricity supply in a motor car) is not provided. Customer safety will not be affected by this restriction.

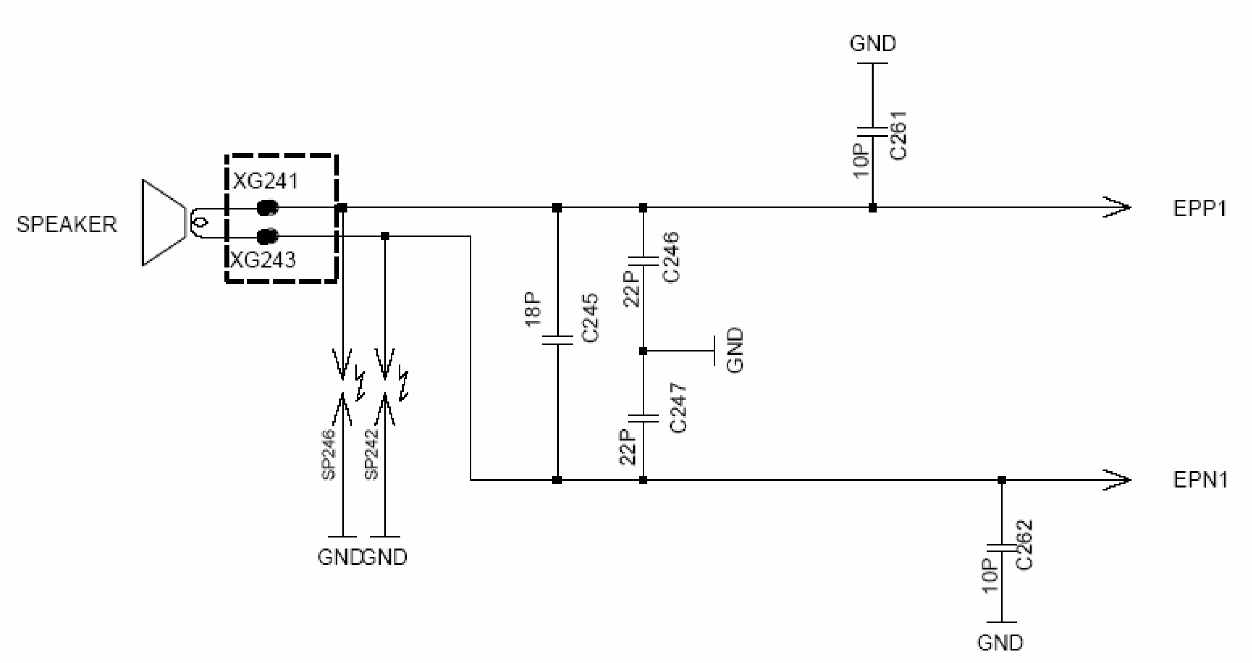
9 Interfaces

9.1 Vibra (XG220)



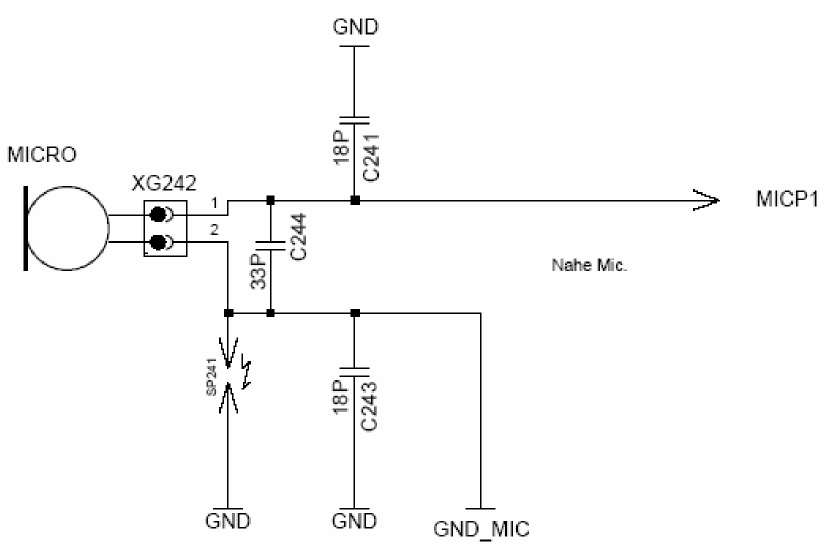
Pin	IN/OUT	Remarks
1	I	BATT+
2	O	The FET V211, switching this signal, is controlled via the EGOLDLite signal VIBRA_UC.

9.2 Earpiece (XG243)



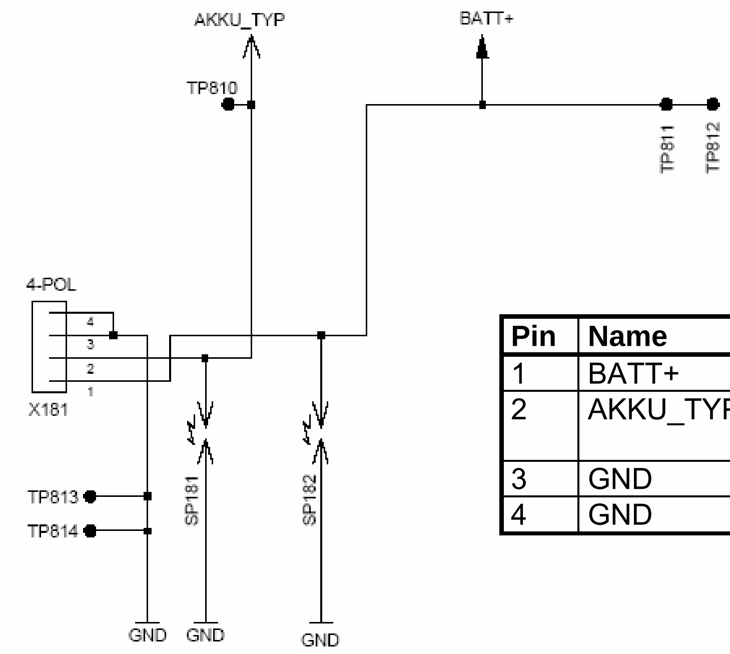
Pin	Name	IN/OUT	Remarks
1	EPP1	O	1st connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation. EPP1 builds together with EPN1 the differential output to drive the multifunctional "earpiece" (earpiece, ringer, handsfree function).
2	EPN1	O	2nd connection to the internal earpiece. Earpiece can be switched off in the case of accessory operation.

9.3 Microphone



Pin	Name	IN/OUT	Remarks
1	MICP1	O	Microphone power supply. The same line carries the frequency speech signal.
2	GND_MIC		

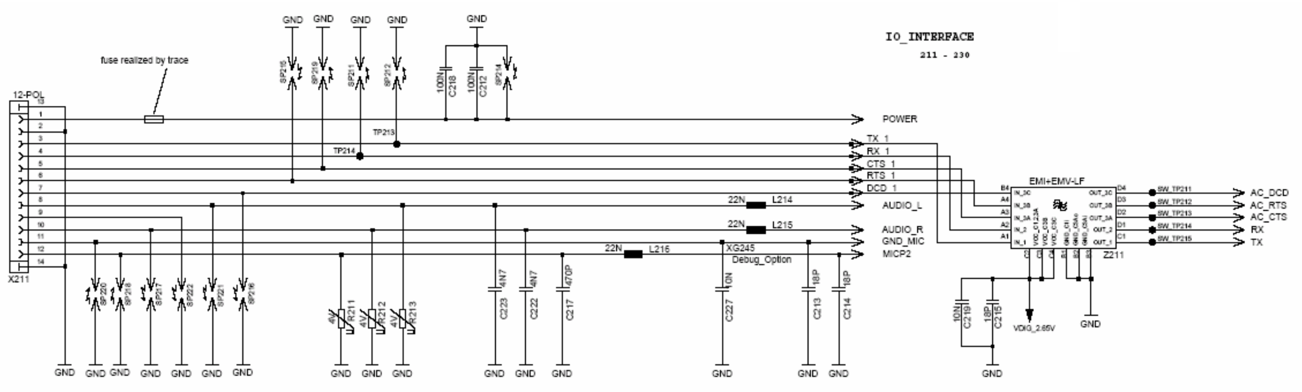
9.4 Battery (X181)



Pin	Name	Level	Remarks
1	BATT+	3 V... 4.5V	Positive battery pole
2	AKKU_TYP	0V...2.65V	Recognition of battery/supplier
3	GND	-	Ground
4	GND	-	Ground

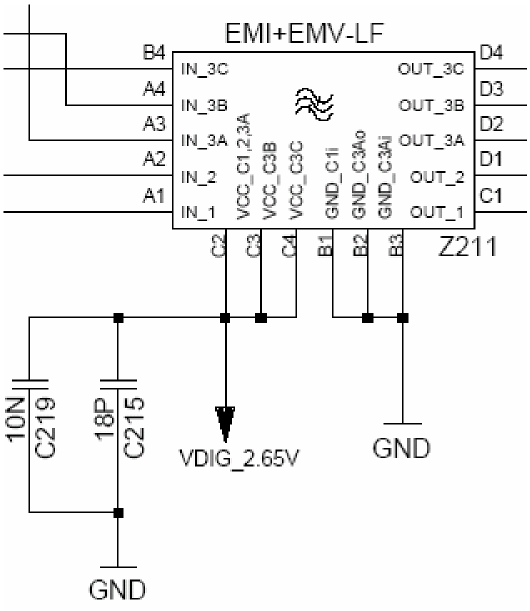
9.5 IO Connector (X211) with ESD protection (Z211)

IO Connector



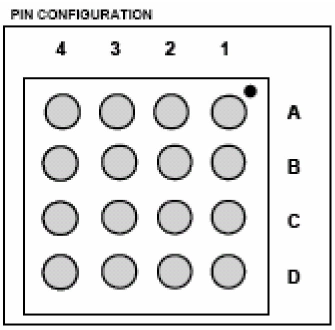
Pin	Name	IN/OUT	Notes
1	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
2	GND		
3	TX	O	Serial interface
4	RX	I	Serial interface
5	DATA/CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
6	RTS	I/O	Use as RTS in data-operation.
7	CLK/DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
8	AUDIO_L	Analog O	driving ext. left speaker With mono-headset Audio_L and Audio_R differential mode
9	GND		
10	AUDIO_R	Analog O	driving ext. right speaker With mono-headset Audio_L and Audio_R differential Signal
11	GND_MIC	Analog I	for ext. microphone
12	MICP2	Analog I	External microphone

ESD Protection with EMI filter



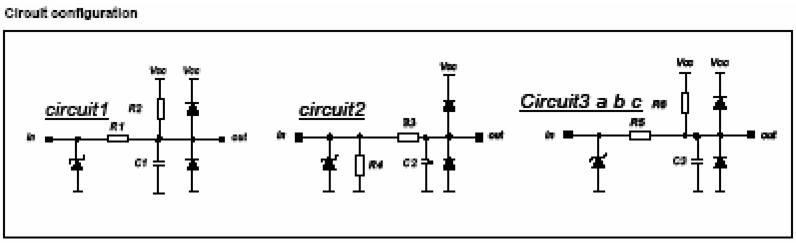
The Z211 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z211 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages up to 8 kV.

Pin configuration of the Z211

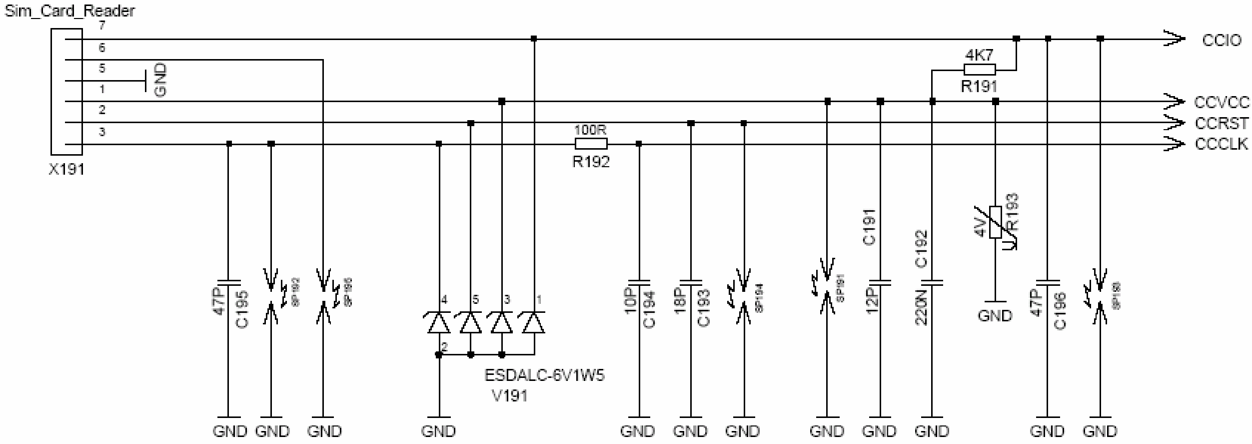


A1	Input C1	C1	Output C1
A2	Input C2	C2	Vcc C1 / C2 / C3A
A3	Input C3A	C3	Vcc C3B
A4	Input C3B	C4	Vcc C3C
B1	GND C1I / C1o / C2o	D1	Output C2
B2	GND C3Ao / C2I	D2	Output C3A
B3	GND C3AI / C3BI / C3Bo / C3CI / C3Co	D3	Output C3B
B4	Input C3C	D4	Output C3C

Z211 Circuit Configuration



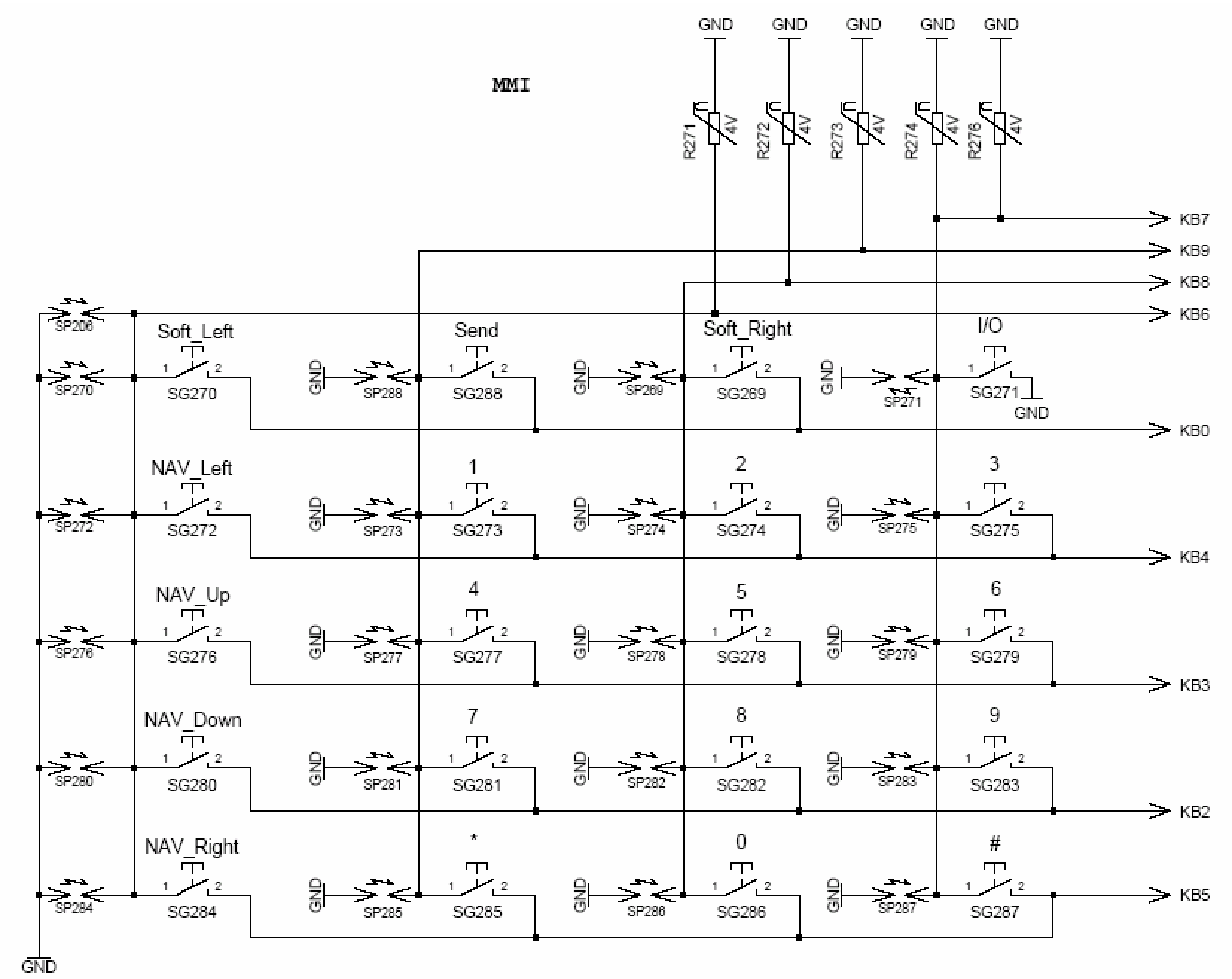
9.6 SIM



Pin	Name	IN/OUT	Remarks
3	CCLK	O	Pulse for chipcard. The chipcard is controlled directly from the EGOLDlite.
2	CCRST	O	Reset for chipcard
7	CCIO	I O	Data pin for chipcard; 10 kΩ pull up at the CCVCC pin
1	CCVCC	-	Switchable power supply for chipcard; 220 nF capacitors are situated close to the chipcard pins and are necessary for buffering current spikes.

10 Keyboard

The keyboard is connected via the lines KB0 – KB9 with the EGOLDlite.
KB 7 is used for the ON/OFF switch. The lines KB0 – KB5 are used as output signals. In the matrix KB6, KB8 and KB9 are used as input signals for the EGOLDlite.



11 A70 IFX Diagram Set

Double click the tag symbol to open the file.

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